IN THE CLAIMS

Please amend the claims as follows.

1-7. (Cancelled)

8. (Currently Amended) An ultrawideband radio frequency signal generator, comprising:

a first signal generator operable to generate a sinusoidal window function;

a second signal generator operable to generate a carrier signal;

a mixer operable to produce an ultrawideband radio frequency product signal as a product of the sinusoidal window function and the carrier signal; and

an RF switch operable to gate the ultrawideband radio frequency output signal;

~~The ultrawideband radio frequency signal generator of claim 7,~~ wherein the RF switch comprises a P-FET, a first N-FET and a second N-FET;

the source of the P-FET coupled to the first voltage source, the gate of the P-FET coupled to the input voltage level, and the drain of the P-FET coupled to the drain of the first N-FET and the gate of the second N-FET;

the gate of the first N-FET coupled to receive the control signal, and the source of the first N-FET coupled to the drain of the second N-FET;

the source of the second N-FET coupled to the voltage reference.

9-22. (Cancelled)

23. (Currently Amended) An ultrawideband radio frequency signal generator, comprising:

a first signal generator operable to generate a sinusoidal window function;

a second signal generator operable to generate a carrier signal; and

a mixer operable to produce an ultrawideband radio frequency product signal as a product of the sinusoidal window function and the carrier signal; and

an RF switch operable to gate the ultrawideband radio frequency product signal, wherein the RF switch comprises at least three coupled CMOS transistors;

wherein the at least three coupled CMOS transistor are coupled to a first voltage source, a voltage reference of a different voltage than the first voltage source, an input voltage level, a control signal, and an output conductor; and

wherein the at least three coupled CMOS transistors comprise ~~The ultrawideband radio frequency signal generator of claim 22, comprising~~ a P-FET, a first N-FET and a second N-FET;

the source of the P-FET coupled to the first voltage source, the gate of the P-FET coupled to the input voltage level, and the drain of the P-FET coupled to the drain of the first N-FET and the gate of the second N-FET;

the gate of the first N-FET coupled to receive the control signal, and the source of the first N-FET coupled to the drain of the second N-FET;

the source of the second N-FET coupled to the voltage reference.

24-29. (Cancelled)